

Scholar All articles - **Recent articles** Results 1 - 10 of about **57,900** for **instruction register decoding**. (0.20 seconds)

Instruction register sequence decoder for microprogrammed data processor and method

HL Tredennick, TG Gunter - US Patent 4,342,078, 1982 - Google Patents

... 27, 1982 [54] **INSTRUCTION REGISTER SEQUENCE DECODER FOR MICROPROGRAMMED DATA PROCESSOR AND METHOD** [75] Inventors: Harry L. Tredennick; Thomas G. Gunter, both ...

Cited by 36 - Related articles - Web Search - All 4 versions

Multiple instruction decoder for minimizing register port requirements

WM Johnson... - US Patent 5,129,067, 1992 - Google Patents

... 7, 1992 [54] **MULTIPLE INSTRUCTION DECODER FOR MINIMIZING REGISTER PORT REQUIREMENTS** [75] Inventor: William M. Johnson, San Jose, Calif. ...

Cited by 31 - Related articles - Web Search - All 2 versions

The SimpleScalar tool set, version 2.0- ►toronto.edu [PDF]

D Burger, TM Austin - ACM SIGARCH Computer Architecture News, 1997 - portal.acm.org

... The **register** fields are all 8 bits, to support extension of the archi ... has a fixed-location, 16-bit opcode field that facilitates fast **instruction decoding**. ...

Cited by 1596 - Related articles - Web Search - BL Direct - All 127 versions

Test generation for microprocessors

SM Thalte, JA Abraham - IEEE Transactions on Computers, 1980 - doi.ieeecomputersociety.org

... for microprocessors at the **register** transfer level. This allows us to treat the microprocessor organization and the **instruction** set as p

Cited by 226 - Related articles - Web Search - Library Search - All 5 versions

[book] Superscalar microprocessor design

M Johnson - 1991 - Prentice Hall PTR

Cited by 666 - Related articles - Web Search - Library Search

Techniques for low energy software- ►york.ac.uk [PDF]

R Mehta, RM Owens, MJ Irwin, R Chen, D Ghosh, E ... - Low Power Electronics and Design, 1997. Proceedings., 1997 ..., 1997 - IEEE Xplore

... This includes all switching in the **instruction register** and **decoder** due to changes in encoding. **Decoder** energy model: Putting it all together: ...

Cited by 89 - Related articles - Web Search - All 3 versions

Instruction control mechanism for a computing system with register renaming, map table and queues ...

J Cocke, GF Grochowski, VG Oklobdzija - US Patent 4,992,938, 1991 - Google Patents

... 12, 1991 [54] **INSTRUCTION CONTROL MECHANISM FOR A COMPUTING SYSTEM WITH REGISTER RENAMING, MAP TABLE AND QUEUES INDICATING AVAILABLE REGISTERS** [75] Inventors ...

Cited by 45 - Related articles - Web Search - All 2 versions

A dynamic instruction set computer- ►ktupm.edu.sa [PDF]

MJ Wirthlin, BL Hutchings - IEEE Symposium on FPGAs for Custom Computing Machines, 1995. ..., 1995 - IEEE Xplore

... The **decode** unit compares the contents of the IR for a ... a new value for the data **register** during the ... Several custom-**instruction** modules of varying size have been ...

Cited by 315 - Related articles - Web Search - All 25 versions

Microprogram Controlled Data Processor for Executing Microprogram Instructions from Microprogram ...

RW Cook - US Patent 3,859,636, 1975 - Google Patents

... means for storing at least a portion of each of the memory words obtained from said main memory; microprogram **instruction register**; **decoding** means connected ...

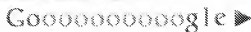
Cited by 26 - Related articles - Web Search - All 3 versions

Y Onishi - US Patent 3,764,988, 1973 - Google Patents

... wherein said fifth means comprises a first gate circuit, responsive to the outputs of said **decoding** circuit and said second **instruction register**, for trans ...

[Cited by 27](#) - [Related articles](#) - [Web Search](#) - [All 2 versions](#)

Key authors: [H Tredennick](#) - [T Gunter](#) - [J Abraham](#) - [M Henry](#) - [J Liptay](#)

Google 

Result Page: [1](#) [2](#) [3](#) [4](#) [5](#) [6](#) [7](#) [8](#) [9](#) [10](#) [Next](#)

[Google Home](#) - [About Google](#) - [About Google Scholar](#)

©2009 Google